REMARKS

Claims 1-4, 7-17 and 22-26 and 28-30 are pending in this application, of which claims 11-17 have been withdrawn from consideration. Claims 1-4, 24 and 26 are herein amended. Claim 27 is canceled. Reconsideration of the rejections in view of these amendments and the following remarks is respectfully requested.

Restrictions

Claims 2, 4, 8, 10 and 23 were withdrawn from consideration due to amendments to specify a second impurity other than boron. Claim 2 has been amended to depend from claim 1. Accordingly, upon allowance of claim 1, the withdrawn dependent claims should also be allowed.

Claim Objections

Claim 26 was objected to because of certain informalities.

Accordingly, claim 26 has been amended to overcome the objection.

Claim Rejections – 35 USC §103(a)

Claims 1, 22, 24, 25 and 27 were rejected under 35 USC §103(a) as being unpatentable over K. Kasai et al (*W/WNx/Poly-Si Gate Technology for Future High Speed Deep Submicron CMOS LSIs*) in view of Jeng et al (U.S. Patent No. 5,877,074).

Claims 3, 7, 9, 26 and 28-30 were rejected under 35 U.S.C. §103(a) as being unpatentable over Kasai et al and Jeng et al and further in view of Tsukamoto (U.S. Pub. No. 2001/0000629).

Applicants respectfully traverse these rejections.

One object of the present invention is to suppress the depletion in the gate electrode of the PMOSFET having the polymetal gate structure. As described in page 5, lines 12-23 of the specification of the present application, the present inventors discovered that the depletion in the gate electrode of the PMOSFET is caused by the fact that boron, a gate dopant of the PMOSFET, is absorbed into the reaction layer between the WN film as the barrier metal and the polycrystalline silicon film to form B-N bonds, which lowers the boron concentration in the polycrystalline silicon film. The depletion in the gate electrode affects characteristics of the MOS transistor and it is desirable to suppress the depletion as far as possible.

Based on the fact, in the present invention, the silicon oxide film and the second polycrystalline silicon film having the thickness thinner than the first polycrystalline silicon film are formed between the first polycrystalline film and the metal nitride film. According to this feature of the present invention, diffusion of boron atoms in the first polycrystalline silicon film toward the metal nitride film can be suppressed by the silicon oxide film and the second polycrystalline silicon film. The thickness of the second polycrystalline silicon film is thinner than that of the first polycrystalline silicon film, so that the increase of the contact resistance between the polycrystalline silicon film and the metal nitride film can be prevented. Thus, the depletion in the gate electrode of the PMOSFET caused by the diffusion of boron atoms toward the metal nitride film can be suppressed without increasing the contact resistance between the polycrystalline silicon film and the metal nitride film.

Kasai et al discloses a method for fabricating a semiconductor device comprising the steps of: forming the 100 nm-thick polycrystalline silicon film on the gate oxide film; forming the 100

nm-thick amorphous silicon film on the polycrystalline silicon film; implanting phosphorus ion and boron ion into the polycrystalline silicon film for the dual gate doping; and forming WN film to suppress the reaction between the polycrystalline silicon film and the tungsten film to be formed on the WN film. In Kasai et al, the amorphous silicon film is formed in order to suppress the mutual impurity diffusion between n^+ and p^+ polycrystalline silicon (see page 19.4.1, right column).

Thus, Kasai et al is similar to the present invention in that the gate electrode includes the two-layer structure of polycrystalline silicon and the metal nitride film. However, Kasai et al clearly differs from the present invention in that the lower polycrystalline silicon film and the upper polycrystalline silicon film have the same thickness, and in that the silicon oxide film is not formed between the polycrystalline silicon films.

Jeng et al discloses a method for fabricating the semiconductor device comprising the steps of forming the polycrystalline silicon layer on the gate oxide layer; forming the undoped amorphous silicon layer on the polycrystalline silicon layer; and forming a tungsten silicide layer on the undoped amorphous silicon layer. In Jeng et al, the undoped amorphous silicon layer is formed between the polycrystalline silicon layer and the tungsten silicide layer in order to prevent the peeling of the tungsten silicide layer caused by the fluorine atoms introduced during the formation of the tungsten silicide layer.

Thus, Jeng et al is similar to the present invention in that the gate electrode includes the two-layer structure of polycrystalline silicon. However, Jeng et al clearly differs from the present invention in that the polycrystalline silicon layer is not doped with boron, in that the silicon oxide

film is not formed between the polycrystalline silicon layers, and in that the metal nitride film is not formed on the polycrystalline silicon layer.

Even if the teachings of Kasai et al and Jeng et al are combined, the combination does not suggest the presently claimed invention. Further, one of ordinary skill in the art would not have combined the references as asserted by the Examiner since there would have been no motivation to make the modifications suggested by the Examiner.

Tsukamoto discloses in the second embodiment a method for fabricating a semiconductor device comprising the steps of: forming the 70 nm-thick amorphous silicon layer on the gate oxide layer; forming the silicon oxide layer on the amorphous silicon layer; forming the 70 nm-thick amorphous silicon layer on the silicon oxide layer; and forming the tungsten silicide layer on the amorphous silicon layer. In Tsukamoto, the silicon oxide layer is formed in order to form the two-layer structure polycrystalline silicon and to crystallize the lower and upper amorphous silicon film into large grain polycrystalline silicon.

Thus, Tsukamoto is similar to the present invention in that the gate electrode includes the two-layer structure of polycrystalline silicon and in that the silicon oxide layer is formed between the polycrystalline silicon layers. However, Tsukamoto clearly differs from the present invention in that the lower polycrystalline silicon film and the upper polycrystalline silicon film have the same thickness, and in that the metal nitride film is not formed on the polycrystalline silicon layer.

As described above, each of the elements of the claimed invention is described in at least one of Kasai et al, Jeng et al, and Tsukomoto. However, as described above, these references clearly differ from the present invention in the objects thereof, constitutions as a whole, and the effects achieved by the constitutions. The constitutions of the inventions described in these references are applied based on the original objects thereof, which are different from each other. Thus, there would have been no motivation to combine the references as asserted by the Examiner.

In the present invention, the silicon oxide film and the second polycrystalline silicon film are formed between the first polycrystalline film and the metal nitride film in order to prevent the above-described problem caused by the metal nitride film. It cannot be derived from the above-described references that the boron diffusion from the first polycrystalline silicon film toward the second polycrystalline silicon film and the boron absorption by the metal nitride film are suppressed by forming the silicon oxide film and the second polycrystalline silicon film between the first polycrystalline silicon film and the metal nitride film.

In Kasai et al, the 100 nm-thick amorphous silicon film is formed on the 100 nm-thick polycrystalline silicon film in order to suppress the mutual impurity diffusion between n^+ and p^+ polycrystalline silicon.

On the other hand, Jeng et al relates not to the dual gate structure but to the single gate structure, so that the mutual impurity diffusion does not occur in the semiconductor device of Jeng et al. In Jeng et al, the thickness of the undoped amorphous silicon film is set to 20-40 nm from the viewpoint of preventing the diffusion of fluorine atoms. It is considered that the undoped amorphous silicon film will prevent the diffusion of not only fluorine atoms but also boron atoms.

However, the diffusion coefficient of fluorine atoms and that of boron atoms are different from each other, so that it would not have been obvious to one having ordinary skill in the art to set the thickness of the second polycrystalline silicon film of Kasai et al to the thickness thinner than that of the first polycrystalline silicon film or to 2-20 nm in order to prevent the mutual impurity diffusion or the diffusion of boron atoms based on the disclosure of Jeng et al.

In Tsukamoto, the silicon oxide film is formed between the polycrystalline silicon films in order to form the two-layer structure polycrystalline silicon and to crystallize the lower and upper amorphous silicon film into large grain polycrystalline silicon. According to this, the diffusion of fluorine atoms from the tungsten silicide film is suppressed, and the fluctuation in the threshold voltage caused by the boron penetration into the substrate due to the effect of diffusion of fluorine atoms can be prevented (see paragraphs [0027] and [0028] of Tsukamoto).

On the other hand, in Kasai et al., the tungsten nitride film and the tungsten film are formed by sputtering method, so that the fluorine atoms are never introduced into these films. Thus, it would not have been obvious to one having ordinary skill in the art to form the silicon oxide film between the first and the second polycrystalline silicon films of Kasai et al to suppress fluctuation in the threshold voltage.

As described above, Kasai et al, Jeng et al and Tsukamoto are clearly different from the present invention and do not provide any motivation for the present invention. Thus, the present invention would not have been obvious to one of ordinary skill in the art, even though these references are considered.

Thus, the 35 USC §103(a) rejection should be withdrawn.

It is submitted that nothing in the cited references, taken either alone or in combination, teaches or suggests all the features recited in each claim of the present invention. Thus all pending claims are in condition for allowance. Reconsideration of the rejections, withdrawal of the rejections and an early issue of a Notice of Allowance are earnestly solicited.

If, for any reason, it is felt that this application is not now in condition for allowance, the Examiner is requested to contact Applicant's undersigned attorney at the telephone number indicated below to arrange for an interview to expedite the disposition of this case.

In the event that this paper is not timely filed, Applicant respectfully petitions for an appropriate extension of time. The fees for such an extension or any other fees which may be due with respect to this paper, may be charged to Deposit Account No. 50-2866.

Respectfully submitted,

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